MAIL ROOM JUL 9 1991 PAT. & TRADEMARK OFF.

B-24314C2

#8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MAIL ROOM JUL 10 1991 PAT. & TRADEMARK OFF.

	JOSEPH T. EVANS, JR. ET AL.
Serial No.:	582,672
Filed:	September 14, 1990
Group:	233
Examiner:	Alyssa H. Bowler
For:	NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

RECEIVED
JUL 11 1991
GROUP 230

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

DECLARATION OF DALE B. NIXON

I, Dale B. Nixon, of 3519 Brookline Lane, Dallas, Texas 75234, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

I.

1. I am a patent attorney, Registration No. 28,454, registered to practice before the U. S. Patent and Trademark Office, and in good standing as an attorney licensed to practice law in the State of Texas.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 8, 1991
(Date of Deposit)
Roger N. Chauza, Reg. No. 29,753
Name of applicant, assignee, or Registered Representative
Roger N. Chauza
Signature
July 8, 1991
Date of Signature

2. On or about November 6, 1986, I visited the offices of Krysalis Corporation at Albuquerque, New Mexico, and discussed the structure and operation of several inventions with various inventors. Pages 1-18 of Exhibit A, attached hereto, are copies of a transcription of a taped conversation I had with Mr. Richard H. Womack on November 6, 1986, in which various nonvolatile ferroelectric memory structures were discussed. The magnetic tape on which our conversation was recorded was transcribed by secretarial personnel at the law firm of Richards, Harris, Medlock and Andrews. It is believed that within several days after my return from my visit to the Krysalis offices, my taped conversation with Mr. Womack was transcribed into the typewritten pages of Exhibit A. The drawings attached to Exhibit A were the drawings discussed during our conversation on such date. Although my first statement on page 1 of Exhibit A indicates that the subject matter discussed relates to my office file B-23727, the material was used in preparing a patent application pertaining to my office file B-24314.

3. Among the various ferroelectric memory cell architectures discussed with Mr. Richard Womack according to the conversation transcribed in Exhibit A, we discussed the one-transistor, one-capacitor configuration, as noted at page 2 thereof. It is further noted in the middle of page 2 that the capacitor can store two states, each of which generates a different charge which can be converted to a voltage by using a sense capacitor. Then, the converted voltage is sensed by a conventional voltage amplifier which is easy to build.

At about the middle of page 3, Mr. Womack states that Krysalis then had two-by-two arrays of transistors on silicon and that they are putting ferroelectric capacitors on the silicon. Mr. Womack further states that testing of the two-by-two arrays is a matter of a couple of days away.

At page 5 of Exhibit A, Mr. Womack describes the reading and restoring of data from an array of single-transistor, single-capacitor cells as shown in Figure 3 of the drawings attached to Exhibit A.

At pages 6 and 7 of Exhibit A, Mr. Womack briefly describes the difference between the electrical charges read from the single-transistor, single-capacitor cell, depending on the polarization state stored therein.

At about the middle of page 9 of Exhibit A, Mr. Womack notes the restoring operation occurring with respect to the Figure 4 waveforms.

At the bottom of page 17 of Exhibit A, Mr. Womack contrasts the sensing and amplification with respect to the single-transistor, single-capacitor memory architecture relevant to Figures 3 and 4, and that of the complementary cell architecture of Figures 11 and 14.

In my conversation with Mr. Kinney, as noted on transcribed pages 19-24 of Exhibit A, we discussed Figure 17 of the attached drawings. The sensing circuit of Figure 17 is connected to a bit line of a ferroelectric memory cell for sensing current that is transferred by the ferroelectric capacitor to the bit line during read operations.

4. The nonvolatile ferroelectric memory cell identified in Figure 11 of the drawings of Exhibit A was also discussed with Mr. Womack on or about November 6, 1986. This type of memory cell is of the complementary type architecture, including a word line WL1, and first and

second complementary bit lines BL1 and BL1 bar coupled to a differential sense amplifier. One memory cell, of which there are two shown in Figure 11, includes first and second ferroelectric capacitors (C_1, C_2) each with first and second plate electrodes. The first (or bottom) plate electrode of capacitor C_1 is coupled to a bit line (BL1) by an access transistor, while the first (or bottom) plate electrode of the second ferroelectric capacitor C_2 is coupled to a complementary bit line (BL1 bar) by way of a second access transistor. Each of the access transistors are located within the memory cell. Control terminals of the first and second access transistors are connected to the word line (WL1). When the word line (WL1) is actuated, the access transistors couple the respective ferroelectric capacitors C_1, C_2 to the respective bit lines BL1 and BL1 bar. A differential sense amplifier is responsive to the difference in voltage between the first and second bit lines. Each ferroelectric capacitor C_1, C_2 has an upper, second plate electrode, each of which is connected to a plate line DL1. The plate line DL1 is distinctive from the bit lines BL1 and BL1 bar.

5. On or about November 6, 1986, I conducted a taped conversation with Mr. Wayne Kinney, an employee with Krysalis Corporation. The transcribed conversation appears on pages 19-24 of Exhibit A. According to Mr. Kinney's statement on page 24, his responsibility at that time was to characterize the electrical properties of the Krysalis developed ferroelectric material and provide Mr. Womack, the circuit designer, with the electrical properties of the material so that he could complete the cell design.

6. During March 1987, I reviewed the invention disclosure material and commenced preparation of a patent application on the subject matter previously discussed with Mr. Womack. I believed that the single-transistor, single-capacitor type of ferroelectric memory cell architecture and the complementary ferroelectric cell architecture were directed to one invention and thus prepared a single patent application covering both embodiments. I prepared informal drawings of the various ferroelectric memory architectures and waveforms and forwarded the same to Mr. Joseph T. Evans, Jr., of Krysalis Corporation, on March 10, 1987, for review. Attached hereto as Exhibit B is my cover letter of transmittal. The cover letter of Exhibit B references my file number B-24314, which is the file of the parent of the above-captioned continuation patent application.

7. After preparation of a draft patent application on the above-captioned patent application, I forwarded such draft application and drawings to Mr. Joseph T. Evans, Jr., as indicated in my cover letter, dated March 23, 1987, a copy of which is attached hereto as Exhibit C.

8. Exhibit D is a copy of a facsimile transmission to me from Krysalis Corporation, reciting revisions to the draft patent application believed to be made by Mr. Joseph T. Evans, Jr. The facsimile letter was forwarded to me by way of telecopy services on March 26, 1987, and believed to be in reply to my correspondence and enclosures identified in paragraph 7 above.

9. After revising the draft application according to the suggestions noted in the Krysalis facsimile letter sent to me on March 26, 1987, I forwarded a revised draft application to Mr. Joseph T. Evans, Jr. on April 8, 1987. Exhibit E is a copy of my cover letter forwarding the revised draft application to Mr. Joseph T. Evans, Jr.

10. Mr. Evans and Mr. Womack of Krysalis Corporation provided me with further comments and changes to be made to the draft patent application. After having made such changes, I forwarded yet another draft patent application to Mr. Joseph T. Evans, Jr. on May 5, 1987. Exhibit F is a copy of my cover letter forwarding the draft application to Mr. Evans.

11. On May 12, 1987, I forwarded to Mr. Joseph T. Evans, Jr. the text and formal drawings of the patent application. Exhibit G is a copy of my cover letter to Mr. Joseph T. Evans, Jr., forwarding such material to him, and indicating the transmittal of the claims at a later time.

12. Exhibit H is a copy of my cover letter, again to Mr. Joseph T. Evans, Jr., in which I forwarded to him the complete patent application, including claims, for signing by the inventors.

13. After discussing with Krysalis personnel yet other changes to be made in the application, I incorporated such changes therein and forwarded a final draft of the application to Mr. Joseph T. Evans, Jr. on May 28, 1987. Exhibit I is a copy of my cover letter of May 28, 1987.

14. On June 2, 1987, I forwarded the executed patent application on the above-referenced subject matter to the United States Patent and Trademark Office for filing. Exhibit J is a copy of my cover letter addressed to the Honorable Commissioner of Patents and Trademarks, for transmittal of the patent application for filing.

15. The correspondence of the above-referenced Exhibits B, C and E-J are referenced according to my office files with the designation "B-24314". The patent application associated with my file number B-24314 was filed in the U. S. Patent and Trademark Office on June 2, 1987, and accorded Serial Number 057,100, as indicated on the Patent Office filing receipt, a copy of which is attached hereto as Exhibit K. The above-captioned patent application is designated "B-24314C2", because it is a second continuation of the parent application filed on June 2, 1987.

16. While the foregoing exhibits identify the correspondence between myself and Krysalis Corporation with respect to the parent of the above-captioned patent application, Exhibits L-O identify the nature of my legal services provided to Krysalis, and the respective dates on which services were provided with respect to the parent application of the above-captioned patent application, i.e., office file "B-24314".

17. Exhibit L is my billing statement for the month of March, 1987, identifying the legal services provided to Krysalis Corporation with respect to my file B-24314. As noted in Exhibit L, I performed legal services in connection with drafting the patent application between March 6, 1987,

and March 23, 1987. During such dates, telephone conversations were conducted with Mr. Joseph T. Evans, Jr., an inventor of the subject matter of the captioned application.

18. Exhibit M is my billing statement for legal services provided to Krysalis Corporation during the month of April, 1987, in connection with my file B-24314. On April 6, 7 and 8 of 1987, I worked on the parent of the captioned patent application by further drafting the application and claims. As further noted in the billing statement, telephone conversations were conducted with Krysalis personnel on February 17, 1987; March 3, 10, and 16, 1987, in connection with the B-24314 patent application.

19. Exhibit N is my billing statement for the month of May, 1987, for legal services provided to Krysalis Corporation. On May 5, 6, 7, 12 and 13 of 1987, I further revised the B-24314 patent application, drafted additional claims and otherwise placed the application in condition for approval by the inventors. On May 14, 1987, I discussed inventorship issues with Mr. Joseph T. Evans, Jr. On May 18, 1987, I had a further telephone conversation with Mr. Evans, in which revisions and modifications to the patent application were discussed.

20. Exhibit O is my billing statement for legal services provided to Krysalis Corporation during the month of June, 1987. As noted in Exhibit O, I drafted further claims for the B-24314 patent application on May 28, 1987. On such date, I prepared signature papers, and I forwarded the application and formal papers to Krysalis Corporation for signing by the inventors. As further noted in Exhibit

O, I talked to Mr. Womack on May 5, 1987, and to Mr. Evans on May 18 and 19 of 1987, concerning the B-24314 patent application.

21. The billing statements of Exhibits L-O are records maintained in the normal course of business at the law firm of Richards, Harris, Medlock & Andrews, now Richards, Medlock & Andrews of Dallas, Texas. The billing statements of Exhibits L-O were made by person's knowledge of, or made from information transmitted by a person with knowledge of, the acts or events appearing on the billing statements. The billing statements of Exhibits L-O were made on or near the time of the acts and events appearing on them, and it was and is the regular practice of Richards, Medlock & Andrews to make such billing statements, and such billing statements were kept in the course of a regularly conducted business activity.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: July 5, 1991

Dale B. Nixon
Dale B. Nixon
Registration No. 28,454

Exhibit A

GLOBAL 1. KRYSLUS TO KRYSALIS
2. D ram to DRAM
3. fero electric to ferroelectric

DISCLOSURE MATERIAL BEING TAKEN AT KRYSLUS CORPORATION IN ALBUQUERQUE ON NOVEMBER 6, 1986 WITH RICHARD WOMACK

The first material that we will cover in the disclosure is the one for file Krys B-23727 which is entitled "Thermoelectric memory cell configurations." I guess the first part is starting with the basic three element cell.

The cell is actually two elements. The third element is the most common of what we consider the best approach in being able to utilize the memory cell.

This is the sense capacitor?

Yes there is one of those per column.

Okay I was under the impression that this was a 3 element cell but we were talking about

using only one cell at a time it basically if you have a memory array there is one of those per column within the array.

We are down to like a D ram with ~~the~~ a capacitor and a single access transistor?

Its very similar to a D ram in that respect, the difference being fundamentally that in a D ram you store two different voltages upon the same capacitor value to render a charge differential when you go to read it. In our case we have the same voltage across that we charge a capacitor with the capacitor having two different values and causing a charge differential that we sense.

This is CFE is the fero electric capacitor

has two stable stakes that effectively give it two different values of capacitance effective values of capacitance and when you switch that capacitor through the same voltage charge you get out depends upon which stable state it was stored in in the previous write into it.

when you are saying two states are these just the most extreme states you can get its actually an analog

its actually an analog device but we are using it in a digital mode. The two most extreme states

you are trying to saturate it then? is that right?

thats close. We are trying to make those two states as large as possible in order to increase our noise margin if you did it in an analog fashion or if you did multiple bits per state its just like a D ram combinations there and you could store more than 1 bits per more information than one

bit per cell same way here except its just D ram is not practical to do that. It would be practical for us to do it depend upon how much signal we have. If we had more signal it would be pratical to do that.

But you are probably trying to get your capacitor as small as possible and thats the other tradeoff right.

right. that has indirect implications on architecture but it doesnt' have direct implications of this signal that you get out. This signal that you get out is determined by not the size of the capacitor but by the ratio of the two capacitance values that you get out. Two capacitance values that the ferroelectric capacitor can have. Not to say that the sense capacitor doesn't effect the signals that you see it affects it does do that but the this ratio of the two capacitances stored in the ferroelectric determines your signal what I've started out doing is talkign about just the basic one transistor, one capacitor configuration and showing how when you depend upon the two states you would get a differential charge out of it. That charge the way you in conventional schemes you have voltage amplifiers are easy to build. So to convert a fixed charge to a voltage you apply it to a capacitor and that ends up being a known voltage that and in this case a voltage differential that you can sense. Thats the significance of the sense capacitor. There are its possible to come up with other schemes that don't have a linear capacitor or a fixed capacitor or it could be a resistor and the charge turns into a current momentary current that you would have to sense. Its possible its not as practical way in semiconductor technology. But there is not anything fundamental about that having to be a capacitor it could be a resistor. Then the next thing I say is I feel like that from a fundamental standpoint most of the ferroelectric methodologies out there all of them that I am aware of are standalone ferroelectric methodologies they don't integrate the silicon technology with the ferroelectric technology.

even on the same chip?

Yes. by just saying chip this integrates it into the memory cell. It may have been thought of before but no one could do it before and that is the significant thing here is that we know how to integrate the ferroelectric technology with the silicon technology to make a memory cell that has a silicon some sort of silicon whether its moss or bipolar

transistor and a ferroelectric capacitor to make it look like a D ram memory cell. As opposed to a pure cross point array of ferroelectric capacitors. That is the first level of significance to me thats what fundamental.

Do you know what it is that makes it now possible for you to do that? that looks like thats a real jewel there.

Its a fact that we know how to deposit thin semiconductor processing is a thin film technology. We know how to do thin film ferroelectric materials that do not or at least they are solvable the problems are solvable as far as chemical compatibility.

compatible with silicon?

yes. its possible for you the chemistry to be wrong since its not compatible. We know how to do the thin films that are not incompatible.

You had actually built deposited these films and tested them and it works on silicon?

We yes on silicon. Yes. In conjunction with the transistor we have a test vehicle now that we've got and we haven't tested it but thats a matter of another day or so. Of where we have this structure on silicon or actually a more complex one than that we have small two by two arrays of these things.

You are getting ready to test those pretty soon?

We have the silicon wafers now with the silicon transistors and we are putting on ferroelectric capacitors on them now?

You bought them from somebody else?

Yes. Thats the most fundamental that says ferroelectric integrated in with silicon. The next level up from there is ferroelectric and the MOS transistor or a memory cell with a ferroelectric capacitor with a transistor. It is possible to have ferroelectric and silicon at the same time but not both of them in the memory cell. To my knowledge not only thats the next level tear down of being fundamental is having the transistor and the ferroelectric in the memory cell. It looks like a D ram cell but the fact is that it is a ferroelectric cell and its a nonvolatile cell in the fact that you have a nonvolatile cell with only two components that with one of them being ferroelectric is the other approaches the people the other approaches that I know of don't include the ferroelectric and silicon at the same time and they don't include

therefore the ferroelectric and the transistor at the same time. It puts not having the transistor puts constraints upon the characteristics of the ferroelectric. Therefore if you didn 't have the ability to add transistors that puts more constraints on the ferroelectric and makes it more difficult to build. So having the transistor in the cell is important too.

Otherwise you would have to have two different fabrications and devices somehow wire them together.

Kind of like a hybrid but its not only have we got one with the same chip we got them in the same memory cell which freeze up like I said freeze up some of the constrants on the building the ferroelectric.

As I understand what you want to do is the thinner the ferroelectric gets the less voltage you have to work with to set it.

Thats a potential parameter that we have to improve upon. But as far as the memory cell goes thats not a constraint on the memory cell?

its not.

Not fundamentally its a constraint where the voltage comes in is your ability to semiconductor technology can only stand so much voltage for any given level of geometry. The swell of geometries the less voltage you can stand. Therefore to be able to scale better and to get higher density we want to be able to decrease the amount of level it takes to write into the memory cell. That you got a memory cell even if you don't accomplish that. We've got the voltage low enough that we can make to state of the art in production semiconductor technology we can get down there if we want to scale further we have to improve the characteristics more but thats more of a marketing/density element as opposed to fundamental can you build.

What you are really trying to get down is have a 5 ? part?

We'd like a 5 volt part and thats exactly right. We ain't got there but we can built a part. We are at low voltage.

Just pump to get the voltages?

right. The next level is

which figure are you referring to now?

that was basically Figures 1-3. The next level is how do you in particular go about utilizing the taking advantage

of the ferroelectric in the cell and being able to turn it into a practical ability to actually get your data out?

Are you going to be referring to all of the DL1 WL1 that type of thing now? figure 4? How would you the simplest way referring to our little figure 1 here how would you read that do you have to put a pulse on it or something?

The

I hope I'm not getting ahead.

Okay. Thats what I was going to talk about. In of the different configurations there are various ways of pulsing to get the data out. Various pulses schemes have advantages and disadvantages. An example of a pulsing scheme is given in Figure 4. That applies primarily to Figure 3 the only difference between Figure 3 and Figure 1 is the fact that Figure 3 has two shows two memory cells on a problem to dramatize how a problem would look. Other than that its the same memory cell. In the way you get data out of it you precharge BL which is the bit line to some voltage you either probably either high or low in MOS technology it needs to be precharged low. Or at the value of the substrate. The value of the substrate is the value that needs to be precharged at this in either case. the reason why that is is the voltage on V1 and V2 in Figure 3 when they are left idle for a long time will there is a reverse bias junction to the substrate on those nodes

Is from the transistor M1 and M2?

right. from the source drain transistors M1 and M2.

What is V1 and V2 again?

thats just a label on that node. And those nodes if left idle for a long time which is a possible thing since this doesn't require refreshing you don't have to access it you can leave it idle. And if they are left idle those nodes will eventually discharge to the substrate voltage or one threshold voltage of a MOS transistor below the word line. WO1 and WO2.

Do you hold a charge on the word lines?

We typically the simplest configuration of operation is with the substrate grounded and the word lines grounded. Which case the nodes V1 and V2 when they discharge the substrate they discharge the ground and the we don't develop any voltage across and do it. If we took the substrate negative for example V1 and V2 would discharge to a negative voltage. That would develop some voltage across the

capacitors and hold it there. That is if the capacitor doesn't have a threshold voltage associated with its operation its larger than than voltage that you discharge that you put across it then it will lose its data. So I recommend on a situation where you don't force cells to be cycled at a minimum time frame that the precharge voltage on V1 and V2 the same as the substrate voltage.

the precharge?

The voltage at which you take these two right before you unaddress the cell so that voltage goes there and stays there and doesn't move. This is kind of under the assumption also that the value that you take the drive lines and the bit lines to you precharge them to is that same. Otherwise drive line is DL1. The bit line is BL. Otherwise you develop some sort of voltage across that capacitor in a steady state condition.

You would prefer not to have a voltage across the steady state.

right. thats so that the polarization value will be at either P1 or P0 according to Figure 2. That is a stable state. If if you have some voltage across it it has a tendency to lose its state it goes some voltage across it it has a tendency to go to the opposite polarization state so you lose data. The way to maintain data in this cell is to keep 0 voltage across it and if there is a threshold voltage involved below the threshold voltage the threshold voltage I'm referring to is a voltage at which you could put across the capacitor in which it wouldn't lose its polarization value. Right now I'm assuming that we don't have a threshold but we there are indications that we do have a threshold but these schemes are designed to not take advantage of the threshold or at least a large threshold we may have a small threshold. I'll get into that later. The in this situation the way to address the memory cell is to precharge the bit line no to ground and then switch the drive DL1 and WL the word line whichever one you select high that turns on the transistor and the memory cell and it also causes a voltage divider across the ferroelectric capacitor and the sense capacitor the sense capacitor is much much larger than the ferroelectric capacitor then basically you taken that much voltage across the ferroelectric capacitor it dumps the charge onto the sense capacitor the amount of charge it puts on the sense

capacitor depends upon whether you are in ferroelectric state P0 or P1. P0 taken with a positive voltage across the capacitor will put PS -P0 charge across the sense capacitor if its in the P1 state its PS-P1.

its much less?

its much less.

How do you define your 1 and 0 states now. one state is P1.

whats void?

you are just picking one arbitrary.

its kind of arbitrary and sometimes it seems backwards.

what are you using?

we are using P0 as a 0 and P1 as a 1. But its sometimes that it seems like that makes sense and sometimes you would think that you would choose the opposite just from arbitrary definition standpoint thats the way it ought to be considered is not anything. just arbitrary definition.

just getting back you pull the bit line low and you pull whichever word line you want high as well as the drive line at the same time that turns on the transistor

it makes no difference in the order of one line versus drive line. the difference is maybe some switching speed or something but as far as fundamental operational cell it makes no difference then what happens then the drive line voltage is applied across the series combination of the ferroelectric capacitor and the sense capacitor. Depending on whatever the polarity state is on the ferroelectric capacitor is how much charge you get moved into these sense capacitor. What is the ratio of the sizes of the capacitance now you since the capacitors should be many times larger than

I'm saying assume that then all of the drive voltages essentially develops across the ferroelectric capacitor to first two orders. thats not really I've done some crude derivations that show that the ideal ratio of that shows the tradeoff between size of sense capacitor and the voltage that you get out. because its obvious the amount of charge you get out of the ferroelectric capactior is still governed by the equation Q = CB. where C is the effective capacitance of whichever ferroelectric state it happens to be in. and V is the voltage that you develop across the ferroelectric capacitor. Therefrom a one sense you want to

get more charge out you want to put as much voltage across the ferroelectric capacitor as possible. To the amount of voltage you get across this change get across the sense capacitor is inversely proportional to the size of the sense capacitor. The larger the sense capacitor that translates to larger voltage across the ferroelectric so therefore more charge gets dumped. That translates to a smaller voltage across the sense capacitor and what you want to do in a practical system is maximize the voltage. Which is kind of simultaneous in maximizing the charge and minimizing the system ? there is an optimum in there. You may not be able to operate at optimum but you should know at least where it is. I've done some crude estimates on what the optimum is.

about the same size? 2 to 1?

what it turns out I have a long derivation concerning it thats not long its just a page and a half. It turns out that the optimum ratio of let me define some terms here this is not in this disclosure.

That might be a critical feature we may want to bring that out as to patentability.

The arbitrarily defined some ratios in order to express things more simply. I have an expression called red L which is the ratio of logic which is the ratio of the

what is that term?

ratio of logic.

ratl.

Okay. the definition of rat L is the ratio of the two amounts of charge you would get if you developed a full drive voltage across the ferroelectric capacitors so its PS - P1 divided by PS - P0. As that approaches 1 your signal goes to 0 because that means there is no difference between the two logic steps. Then I have defined the ratio of the sense capacitor to the effective capacitance of a logic 0 state is the other pertinent ratio. In other words PS - P0 divided by times the voltage that times the drive voltage is the divided by the drive voltage is the effect of capacitance of the P0 state. And in the ratio the optimum ratio between it and between the sense capacitor and it with a sense capacitor divided by that capacitance is the square root of rat 1.

what does that end up being? is there a handle

if

I guess it depends on what ratio a charge you want.

it depends upon your ferroelectric capacitance ratio. It depends upon your logic ratio but the ideal what the optimum sense capacitor should be.

I get you.

In other words if you have a very small difference between your logic when you are logic 0 the ideal sense capacitor is very close in value to your logic 0 effective capacitor.

kind of a weak device.

thats ideal in thats ignoring some other design parameters that I'm not sure about what they are yet either. I've got some inklings of some ideas but we are gathering data now we need to get a better handle on them.

if you had a stronger lines forward

if you have a strong device you can have a larger bit line to sell capacitance ratio and still have plenty of signal. AS the drive voltage increases you get more signal and

a long point of getting there but I understand it better.

The after you dump the charge on Figure 4 after the drive line and word line have switched the charge there is some sort of charge out there and you have to figure out whether that represents a logic 1 or a logic 0. Assuming you have some method of doing that you then take some time to do that and restore the bit line to the appropriate value.

Side 2 of tape 1

If you go make a footnote about architecture of Figure 5 not only can you have a choice of ? and 6A and 6B you also have the ability to not switch the drive line at all. In which case if the word line switch is high and for some reason you could keep the bit lines from switching and you could keep the drive lines from switching then there would still be 0 volts across the ferroelectric capacitor and it would still be unaddressed.

could you I didn't catch all of that.

If

referring to figure 5.

right. If you detach the bit lines from the differential amplifier and such that they didn't switch the word line switched and you didn't switch the drive lines then with the 0 volts on the bit lines and 0 volts on the drive lines even with the word line switched there would still be 0 volts across the ferroelectric capacitor and it would still be unaddressed. It would be addressed but it would not have lost its data. So therefore you have the option of multiplexing your columns into the same differential amplifier. So therefore you could have a column select there when it enables you to have fewer differential amplifiers.

you could use one diffamp for all the columns then?

yes. for many columns. Thats an advantage of that type of architecture. But it requires a threshold of several hundred millivolts if you want to use the scheme in Figure 7. It doesn't require a threshold if you use Figure 9 scheme. near as much but if you want to use the high density scheme of Figure 7 then it requires several hundred millivolt threshold. Another architecture that is used to get around the threshold problem and still maintain the density of Figure 7 is shown in Figure 11. And in this figure the drive line is decoded along with the word line and is runs parallel to the word line instead of to the bit line. And therefore

In figure 11 is the top there is that DL 1?

yes. and with the drive line being decoded with the word line and only switching when the word line switches means that the disturb across the ferroelectric only occurs when its addressed which means its not a disturb its a read. so therefore you are back down to the noise immunity or very close to the noise immunity that you get in Figure 9 but you still got the density of Figure 7 and the penalty you have paid is now you are stuck with having to have a diff amp on every column and you can't multiplex the columns into the diff amps. In other words you've paid for it in numbers of diff amps. You have got to have that many diff amps instead of having a choice.

I don't understand the reason. why do you have to have that number?

You can't I don't have it shown in Figure 5 but you can put multiplexing transistors down here at the bottom of the bit lines. Which means you can multiplex your diff amps

among different bit lines assuming that you don't switch the drive lines. In Figure 11 all this drive line switches on all the cells down the word line so therefore you have to have a diff amp in order to restore every cell.

you are only doing restore in Figure 5 for the particular cells you went?

right. particular column. Here in figure 11 you are addressing all the columns and you don't have a choice. go through standard logic means of doing it but its not doesn't buy you anything.

I guess the tradeoff then would be is how many cells can you put on a single column if you have a whole lot of them it really wouldn't matter it would matter less and

and thats determined by the optimum ratio of the sense capacitor to the cell ? the sense capacitor is essentially the parasitic bit line capacitance that you normally have. In that case it puts an upper limit on you. Timing for Figure 11 is shown in figure 12. which case it looks very similar to that in Figure 4. This forces you to have to restore the ones and zeros and series again just like in Figure 6a. in figure 4. So there is nothing new in Figure 12. Figure 13 addresses the problem of just pointing out that of the discussion we had earlier about the optimum ratios. You don't get the full voltage across the ferroelectric capacitor some of it falls across the sense capacitor. Therefore the amount of charge you get out is diminished. Its not PS - P1 - PS - P0 in other words its not P1 - P0 anymore its P1 and prime of this P0. is the amount of charge differential you see. in actuality with the sense capacitor. The other problem associated with this is that we talked about why we went to double ended sensing in other words two cells per bit

that doubles

it doubles your signal it doubles your amount of area hazard density and it allowed the two cells to track we have also found that it not only matters how many times a cell has been addressed but it matter what data was written into it whether they attract or not. If you still keep the two cells per bit or even if you don't keep the two cells per bit lets say you do right now you keep the two cells per bit if the amount of charge you get out when you read a 1 is PS - P1. A 1 is read the reason I chose the nomenclature for 1 and 0 is because a 1 is the cell that was polarized in the

same direction as what you read it in. Therefore a 1 does not get destroyed when you read it the 0 gets destroyed. because it was polarizing in the opposite direction than what you read it. Therefore a 1 if this hysteresis shown in Figure 13 was the way the device behaved and it was a reversible process perfectly reversible process when you read a 1 you would slide up the curve toward PS and then if you bring the drive line back down if you pulse the drive line if you went up and down with the drive line you would slide up and down the curve for P1. What you would do for P0 you would go up to the curve to VR and down the curve to P1'. If you look at the voltage across your differential amplifier for the two cells per bit scan if you use a pulse instead of a step to read your data out with what you would do is for a 1 is if you precharge the bit lines to ground a 1 would go up and then back down to ground if it was totally reversible process. A 0 would go up and back down some but it would not go back down to ground. The amount of charge left on that capacitor for 0 would be your total differential and it would not depend upon a 1 tracking a 0 the 1 cell tracking the 0 cell all that differential depends upon the characteristics of the hysteresis curve of the cell that had the 0 stored in it and it depends upon the reversibility of a 1 that it doesn't depend upon the two tracking at all. Well much much less. So if you in other words if you read whether you use architecture shown in Figure 11 or architecture shown in Figure 5 if you read with the pulse instead of with the step that is shown in Figure 14 thats where we take the drive line high and we bring it back low and then we do our sensing and amplification. Whereas in the previous figures we took the drive line high that are sensing in an amplification restored the 1 which doesn't need to be restored the 1 does not need to be restored then we restored the 0 by taking the drive line low if we take the drive line high and then low and then do our sensing assuming the 1 does not need to be restored we can then just restore the 0 and go about our merry way. It depends upon primarily the characteristics of the memory cell that had the 0 stored in it not any tracking between two memory cells. Saying that allows you to say that within the ability of this a 1 being a reversible process it turns out its not a totally reversible process but the first order it is a reversible process it is a process though not

reversible is more highly predictable is not effected near as much with past history. The 1 the reversibility of the 1 is not as effected as much with the past history so therefore if you can build a reference circuit that takes into account the reversibility of the 1 or lack thereof you can go to single ended sensing if you do a full pulsing scheme because that way your voltage reference is not some dummy cell that has a different history than the cell you are sensing your voltage reference is ground and some offset that is relatively independent of history. Now this is how you can go to single ended sensing is by doing a pulse on the drive line instead of a step.

this is using architecture in figure 11 or does it matter?

either 5 or 11. or just and in the basic it can be used with two cells per bit and it gives a better performance than any other scheme I've come up with for 1 cell per bit. This is a way of eventually evolving to one cell per bit with either architecture 5 or 11 the issue between 5 and 11 is threshold and disturb. As far as tracking of the two cells they have the same requirements. The difference between 5 and 11 is the ? problem. Now figure 15 timing scheme there is an issue between two cells per bit and one cell per bit that two cells per bit are needed in that particular case whether you would use a pulse or whether you would use a step you've got a reference there that has at least been cycled the same number of times. The figure you also got double the signal. You can use the pulse scheme or the step scheme with two cells per bit. with one cell per bit in order to develop a reference you probably need to use the pulse scheme. So the tradeoff there is assuming that you can use the step scheme with the two cells per bit architecture and but you have to use the pulse scheme with the one cell per bit of architecture you have basically a time versus area tradeoff. The pulse scheme takes longer. Has potential to allow you to one cell per bit. So therefore from corporate objective point of view assuming that last statement was true if we decided to put a fast part out we would use the two cells per bit and throw area at the problem achieve time. If we wanted to put a dense part out we would do one cell per bit and use the pulse scheme. I'm debating on our first part with two cells per bit which one I want to use I haven't decided yet. Its

a real question. So they are both important at this time. looks like they be ? The sense amp of figure 15 has a problem. Becuase we have a destructive read because we are sensing charge on a capacitor like a D ram and because the magnitudes of the voltages were sensing at this time are similar it is appears to me that it is wisest to use something like a D ram sense amplifier to do the sensing.

Thats basically what Figure 15 is?

Figure 15 is an example of a CMOS D ram sense amplfier. Its not the one that I'm using I've changed it I saw a problem with this. It similar to the one I'm using. thats the idea to use a D ram sense amplifier as opposed to an S ram sense amplifier or using a resistor or using something like in Figure 17. Figure 16 shows an example timing of the signals of that D ram amplifier.

The one in 15?

right. Other than the timing that we have discussed up through figure 14 there is not anything special about that timing other than the fact that its applied to a D ram sampler you take the timing up through figure 14 and apply standard D ram sense amplifier timing to it and thats what you get in Figure 16. There is not very much of a leap there. Joe seems to think its pretty important that is significant that we are using a D ram sense amplifier. I feel like its the obvious approach. But that wasn't obvious to him and it may not have been obvious to come to think of it it might have been obvious to him he seems to think its significant and I haven't figured out why its so significant.

using a D ram sense amplifier?

The pulsing schemes that we come up with trying to solve the disturb problem and the fatigue tracking problems I feel like are significant whether we use a D ram sense amplifier we could it with an S ram sense amplifier it just wouldn't make as much sense. The figure 17 shows an idea that when Kenny proposed to combat the problem of the optimum I talked about between the sense capacitor and the cell capacitor and this scheme he uses the gain of an inverted amplifier and a capacitor to basically hold the bit line node at a virtual ground level so that the bit line node might change by whatever the sensitivity of the amplifier is 20 millivolts or something is held basically steady. The output of the inverting amplifier would be some

proportional to the amount of charged dumped from the sense capacitor. The reason why I havent' implemented that is because I haven't I feel like the D ram sense amplifier is the obvious way to go.

its the best way you've found so far?

Yes I think so however part of that reasoning has to do with the D ram sense amplifier when if you talk about absolute voltages the only way I know how to build the obvious approach to me to build this inverting amplifier for Figure 17 is to be the transistor that is turned on. To turn on a transistor it takes having some voltage over his threshold voltage and the threshold voltage is a run volt. That means the bit line may be held to a virtual ground but the absolute voltage of that is somewhere over a volt. On a 5 volt system you have lost 20% of your potential switching voltage. If I have enough signal such that I have a bit line to cell capacitance ratio of over 5 I can have I can lose less than 20% of my switching potential across the cell capacitor. On an 8 volt system or a higher voltage system this makes more sense. On a lower voltage system you have to have a special amplifier its code mode range down it at a much lower voltage than what I the simpler approach that I have come up with. It sounds more complex I'm kind of afraid of it I feel like the problem with the idea is not the idea I feel its a problem with me and my ability to implement it. So from if we ever decided to do an analog storage you would probably take something very similar to figure 17 and implement it it will be worth it but a digital storage I feel like its value is marginal. Since its marginal I go with the thing I've got experience with which is something closer to figure 15. Thats my problem not the problem with the circuit. From an analog point of view if we were to analog storage or multilevel storage figure 17 might be the way to do it. Thats looking to the future more. Thats it.

Thats a lot of material there. go back and get a quick summary out of there. Which one of the circuits do you think are the ones that are really the most fundamental or the new or the ones that are significantly different involving the

the fundamental is silicon with a ferroelectric.

putting them all together in one cell right.

I wrote that up simply because I'm the one doing sense amp design and he mentioned that idea and I felt like it was a good idea I didn't feel like I could use it now. somehow I like sticking ideas off of the back of the head and coming back using them. The most fundamental as I said earlier is the fact that we are able to integrate the ferroelectric into standards semiconductor. The second tier is the ferroelectric and the transistor in the same cell. The I think its important to have two cells per bit for cycle tracking.

this is because we are using ferroelectrics

that have memory. where they have been. its more than just a previous cycle. And I think the next most important thing is the architecture of figure 11 that is not the most obvious approach. And

is figure 11 what you will be using?

that what I will be using the first. Then I feel like the pulsing scheme of figure 14 is the next question 14. The next most important thing out of that is architecture in figure 5 and the idea that you can multiplex the sense amps. or the columns. actually address a word line and not switch date line and bit line and nothing happens. thats the next most important idea. Then I think the next one is figure 9. the total isolation.

You are not going to that now?

No we will go to that if we have to. If we have to. Then I feel like Joe thinks the idea of using a D ram sense amplifier is the next most important thing. And he may put it someplace else than where I put it and then I feel like the next one is that of figure 17. There is some things I've mentioned in here like figure 8 for example isn't on the list thats because figure 9 is better in all respects. No figure 9 is slower than figure 8 because its got two transistors in the current path instead of just one. But the vast majority of the respects if you got threshold problem you will stop it with figure 9 or 8. And the timing scheme of figure 6b is not very important. I feel like its kind of supplanted by the idea of figure 14 and the somehow I didn't mention it but just the raw timing scheme mentioned in figure 4 is probably thats more fundamental than figure 14 and figure 14 kind of includes it. So actually that timing scheme is probably higher on the list than figure 14. Its more fundamental.

I think thats important. Briefly mention again the pulsing I caught most of it and I've got it on tape but the pulsing aspect is summarize that again. what we are doing. in figure 6b.

November 6, 1986
Tape no. 2 side 1

We are having a short discussion of figure 14 and the pulsing of the drive line concept.

The other problem other than just number of cycles on how two cells do not track is the data that specific data history that has been written into each one. So the idea behind the pulsing scheme in figure 14 is that to get the 1 to cancel itself so that the full differential is taken from the cell that is had a 0 written into it. The way you do this is you pulse the drive line up and back down and if the 1 retraces itself on the hysteresis curve then there would be no change in voltage on the sense capacitor that was reading the 1 cell. and the entire differential voltage would appear on the sense capacitor of reading the 0 cell. It turns out that its not totally reversible process so there is some small voltage left on the sense capacitor that was reading a 1 but that differential voltage is not at least we don't think so far is sensitive to past history. Therefore you can take it into account easier. So that is the so now with that scheme all you have to worry about that under worse case history that a cell will have a large enough hysteresis curve when referenced to itself you don't have to worry about it tracks the other cell if the 1's cancels themselves I think they will.

this is contrast say figure 4 where we have the drive line it looks like its pulsed but its got to be relative to something when you pull it down.

the difference is when the sensing and amplification takes place. In figure 4 the sensing and amplification takes place while the drive line is high and in figure 14 it takes place when the drive line is returned back to lower ?

we've got

this is all relative all the polarities could be reversed. on everything.

I think I got that now. Any more points. we have covered a lot of material now.

DISCLOSURE MATERIAL TAKING ON NOVEMBER 6, 1986
WITH WAYNE KINNEY

Sense amplifier that is described in figure 17 is very simple its simply a current amplifier rather than a voltage amplifier and

where it says cell here we are talking about the ferroelectric cell?

yes.

we put in the drive line signals through the ferroelectric cell.

yes. and it BL bit line so all of the past transistors and all of the other things that are drawn in these other cells would also be in there between the cell and how many sense amplifier and the only difference is that the standard sense amplifier drawn figure 15 will be replaced by the one in figure 17.

let me get a little better the CS is the sense capacitor which would be for a whole column I take it.

It would be for that column yes but it would be only sensing one cell at a time.

just you've got some switching transistors are shown in here routing ones word line transistors.

right. so the only thing different about 17 is that we've dropped in a different sense amplifier two different amplifier schemes. rather than a current amplifier which I said its really a charge amplifier or charge electrometer basically. Its pretty standard in the state of the art to draw something like that amplifier with feedback in a sense capacitor for a charge measurements. The advantage of this one is that the bit line stays very near ground all during the time even during sensing so that most of the voltage applied across the cell in fact drops across the cell rather than having to have a substantial part drop across the sense capacitor so it allows you to drive at lower voltages and still get a large fraction voltage across the cell.

you are saying make it possible to have the drive line a higher voltage?

the drive line will stay the same voltage but the voltage applied across the cell that is the difference the drive line and bit line will be larger in this case because we don't let the bit line rise up as much we keep it almost at ground.

you are shifting the charge out of the cell and putting it on the sense capacitor and the process of doing that you have got a charge it up so you generate a voltage at the output of the differential amplifier and that voltage is the voltage you are reading instead of sensing the voltage across the sense capacitor like they were showing in the other.

yes. its very similar idea this drawn circuit as shown is not unique you find that in textbooks all over the place.

feedback yes but not using it by for the purpose of sensing a ferroelectric pulsed cell. You havent' built this or tried this?

Not as drawn here although in principle we have done exactly the same thing what I'd done in practice I mixed this very closely is we have an electrometer which is a charge amplifier. We can pulse or wrap very slowly the drive line on the cell feeding directly into the electrometer the voltage at the input electrometer stays grounded get voltage output how much charge is moved thats exactly the same operation as the ? circuit in figure 17.

do you get a greater voltage out of here rather than the way it is charging the capacitor?

No. what you get one of the things that is necessary in order to sense the cell you need to apply enough voltage to get past the course of field the farther past you get the better you get more and more of this remnant charge the remnant charge is the memory. If there is problem right now we are having to drive larger voltages than we would like and even so we are not getting as much of the charge as we would like. Higher voltage you can drive across the cell the more than charge you get out. this is simply a technique that allows you for a given drive voltage basically fixed by the silicon technology at this point. Say at 8 volts our present scheme instead of getting 8 volts applied across the cell when you are trying to do a sensing you only get something like 6 volts. This you could get 8 volts depending on how much gain you wanted to put in the amplifier.

able to stretch the cell more to its capacity than just using the same voltage.

If we have ferroelectric material that has a very square loop so that you dont' have to go above 4 volts in

order to get all the charge out then there is no point in doing that unless you are limited again on my silicon technology you being in the drive only 4 volts in which case it would be wise at that point or useful at that point to have a sense amplifier that would allow you to get all of that voltage across with.

okay. are there any other areas that you particularly worked on? we hit all of these.

the only other things I discussed directly were the two different sensing schemes one where you sense on after only having risen the pulse and the other where you rise up and fall again.

thats figure 16 we talked about that a bit. the pulsing technique for the drive line?

yes. see

Figure 16 I think its the top in DL 1.

yes. in one scheme one would want to sense during the time that DL1 was high and the other you would want to take it high and bring it low and then do your sensing and there is some advantage to doing it when its low the disadvantage is that its much slower you have to wait not only to get the thing fully charged up you have to wait for it to fully discharge so thats very slow. the advantage is that it should be much easier to sense particularly for a single ended cell not using two ferroelectric capacitors in order to make one bit of memory using one this has an advantage in that you are only sensing the remnant part or the memory part rather than the remnant plus the nonremnant or the remnant plus the saturation polarization orignally use. Therefore in single ended sensing where you have to have a very good well known reference and you can't allow your signal to straight past that without it having been memory in that kind of single sensing where you were trying to sense some high level that would mean that not only would the remanant portion of the signal have to stay constant within a certain bounds but the nonremnant portion would also have to stay constant and we know already in fact as you fatigue the cell both of those parts change it becomes difficult in order to make a single ended or a single cell sense with sensing on the high level because the amount of variation in your signal changes drastically as you age it wheres the if you sense that the low part of the signal then only the remnant part is there and then you have to take

account of the variation of the remnant part but thats fairly small compared to the variation in the nonremnant ? the primary advantage of this would be for single ended sense where you are using one ? capacitor bit the disadvantage is that its slower.

Could you go through 16 a little bit and tell me exactly what these steps are here on the side? I know the first one is equalization and that what are you doing during equalization.

Richard will probably help you more with this than I could. He is grounding both of the bit lines I believe.

And the data line we are getting everything to 0 state. Is this second is that an F or an E?

Thats an E for equalization.

Is that a line in one of the circuits? do we show it?

its a line in the sense amp I believe there is a line in the sense amp in figure 15.

which line is it?

E.

that turns on all three of those.

turns all of these on so that this line and line are shored together and they are both shorted to ground.

you are just balancing out the ? whenever the drive line goes high you are dumping the charge from the ferroelectric

before the drive line goes high you put the word line high.

thats the selection

thats the selection that says we are getting ready to address this one particular cell. then the drive line goes high and as it goes high the amount of charge that gets dumped into a sense capacitor either by the scheme on figure 17 or by figure 15. both of those has sense capacitors he hasn't drawn it specifically in figure 15. Both of those cases the amount of charge gets dumped onto that it depends on whether or not you would previously polarize it one direction or the other. Thats the memory part. Then in one scheme one would sense then while you are high double ended which double ferroelectric cell which figure 15 would be the sense amp for. one can sense while its high in the advantage of the advantage of that it is fast. you don't have to wait for things to settle down. As we are drawn in figure 16 rather than sensing there you then drop the

guideline and what that does it makes the non? part of the polarization come back off of the sense capacitor and the only voltage left on the sense capacitor is that which is due to the charge which is remnant. then after that is settled sufficiently you then latch in the sense amp. latching the sense amp is amplify and restore 0. it shows the bit lines drifting up with the sense capacitor the voltage on the sense capacitor and then he says amplify and restore 0 thats where he latches in the sense amp. It drives one of the bit lines to ? Vcc and the other bit line to ?

Okay. get your differential. the discharge is where you discharge that bit line back to 0.

yes.

That occurs whenever equalization goes away.

Yes. the way that this behaves when you yank the sense amplifier bit lines up or down it also restores the data at the same time. It only restores it really goes back and only rewrites only the what we are calling the logic 0 where we flip the polarization it flips it back the one where we hadn't flipped it where we are always polarizing the same direction not trying to flip it during sense its not fully rewriting it it leaves it as it is but we had a partial rewrite during the sense which is sufficient but we are not trying to force some remnant polarization to flip so how could we already left it the same way we don't have to restore it to that extent.

How long does your charge last? if you did nothing to it? indefinitely?

thats something we still need to test to verify, theoretically it should last forever. some we have done some preliminary work and certainly over short periods of time short being half a day it certainly stays one of the other things we've done is if you write something in and simply cycle up and down in temperature one of the possibilities is that certainly what happens you go higher in temperature you lose some of the polarization the question was does it stay lost or does it regain as you cool off again and we found out it doesn't in fact mostly regain lost a little bit but it did regain when we got back to room temperature. Most of it secondly multiple times didnt seem to lose any more whatever we lost was just one shot deal. We haven't done anything to prove real long term memory the expectations of that will not be a problem.

probably no 7 day limit. any other areas here that were particular significance to you?

I don't think so. those were the main things I got involved in.

Where is your primary effort directed?

My responsibility at this point is and doing the electrical characterization of the material to provide both for the ? a response to how well they are doing making the stuff for the properties that we want and provide to Richard the characteristics of the material he needs in order to try to design a memory with this amount of charge and these voltages needed to be applied and all that kind of stuff.

You are really testing this film every time they make it to see what its parameters are?

yes. and one of a less important responsibility although hopefully to become a primary responsibility once we get past some of these milestones is to develop some of the theory to explain why material behaves the way it does.

Is physics your background?

yes. My work experience has been semiconductor devices engineering which is not my background in school.

You can explain exactly why all of this stuff is doing whats its doing.

I can wave my hands above water.

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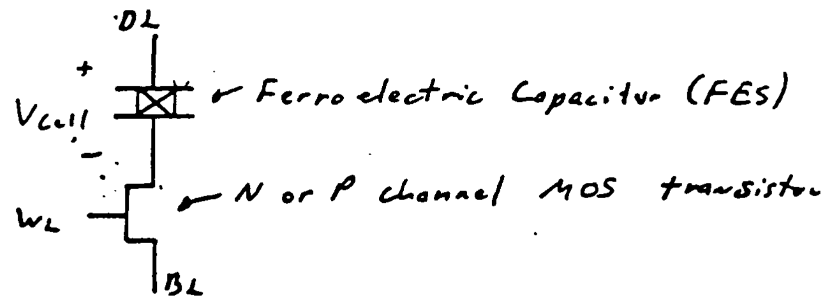

Figure 1

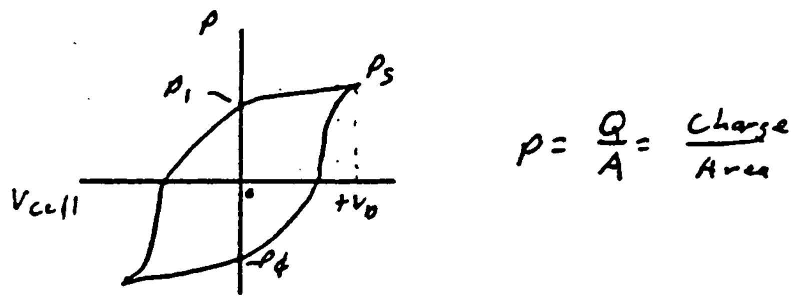

Figure 2

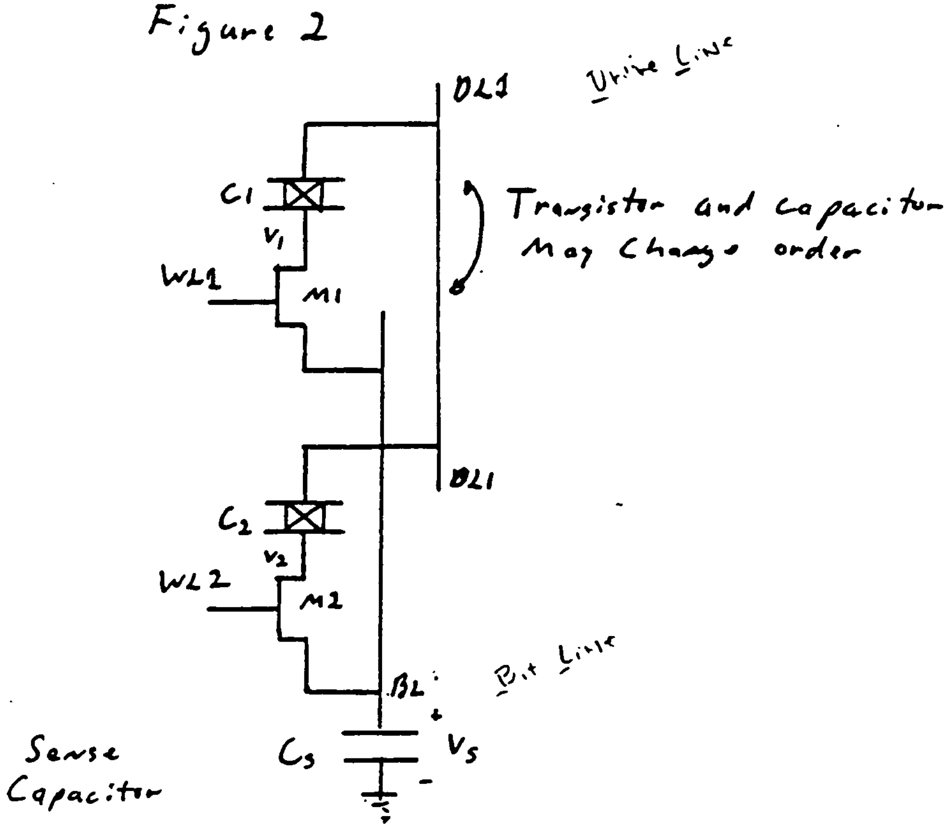

Figure 3

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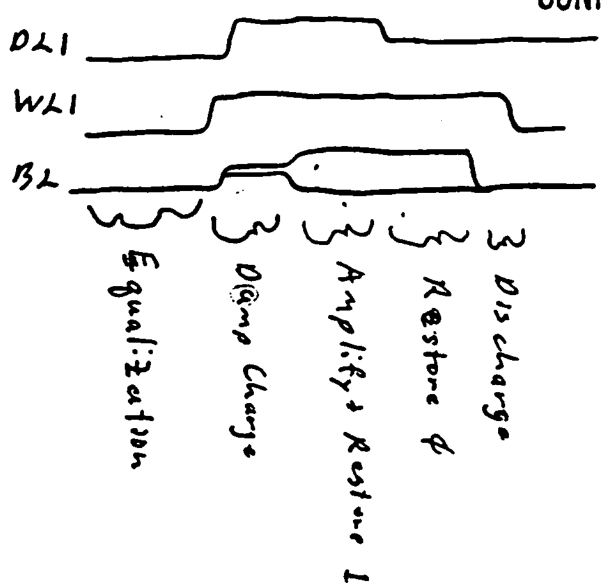

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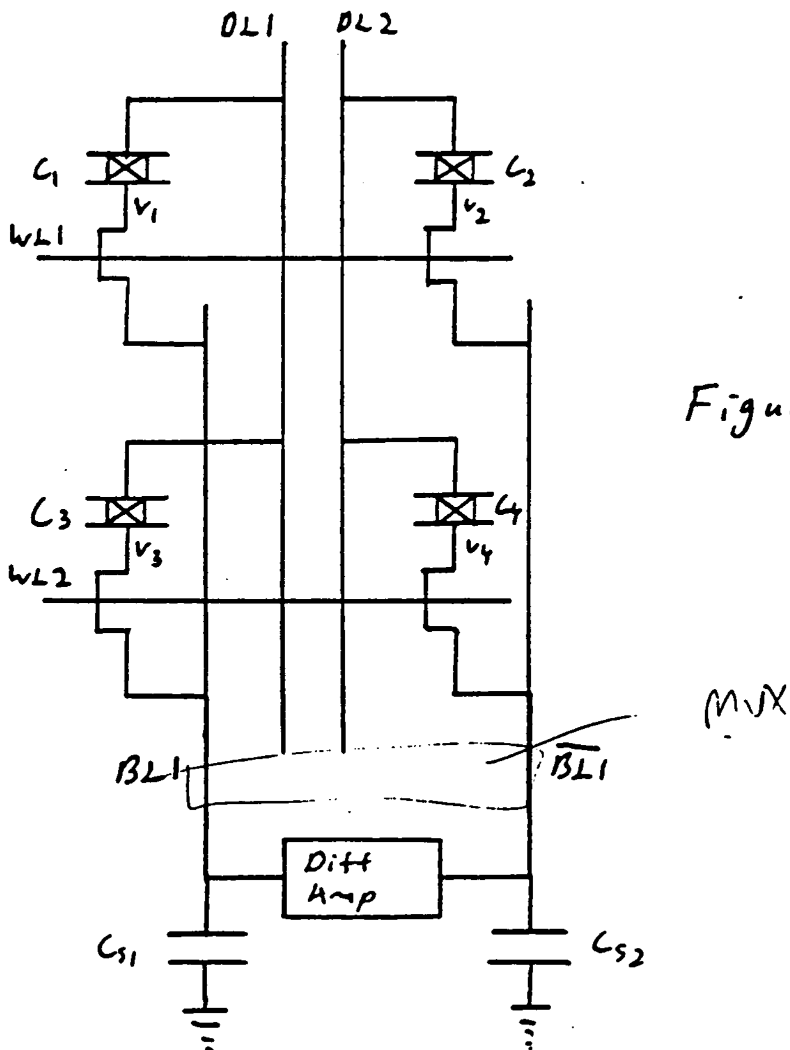

Figure 5

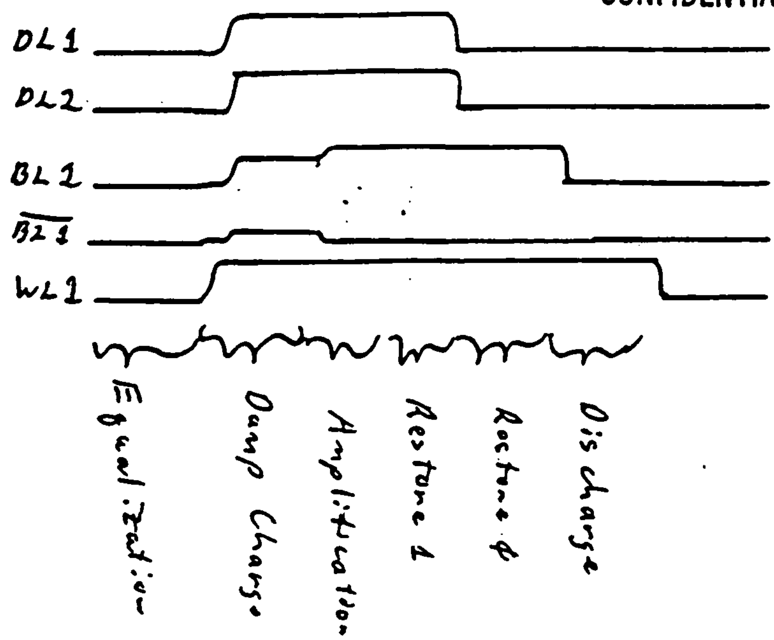

Figure 6a.

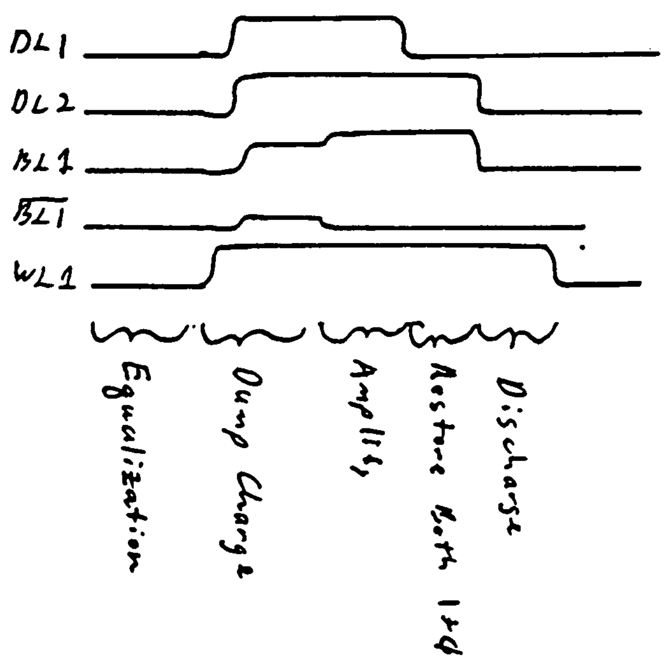

Figure 6b.

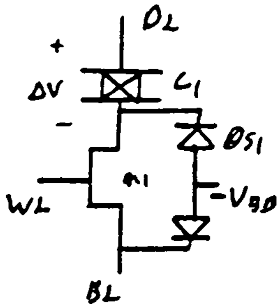

Figure 7

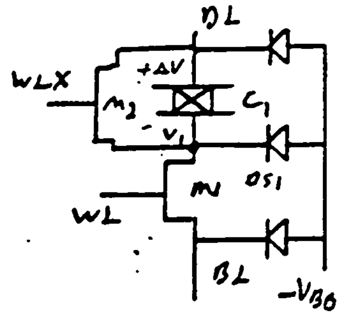

Figure 8

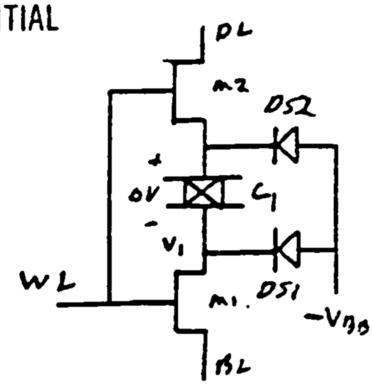

Figure 9

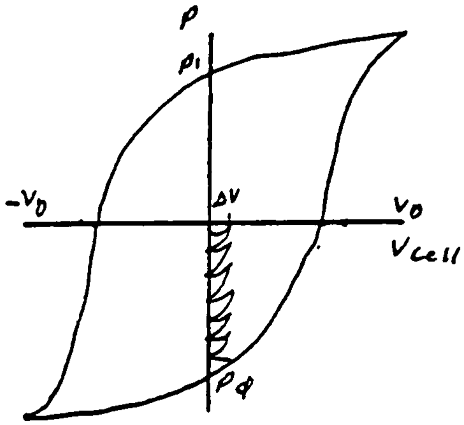

Figure 10

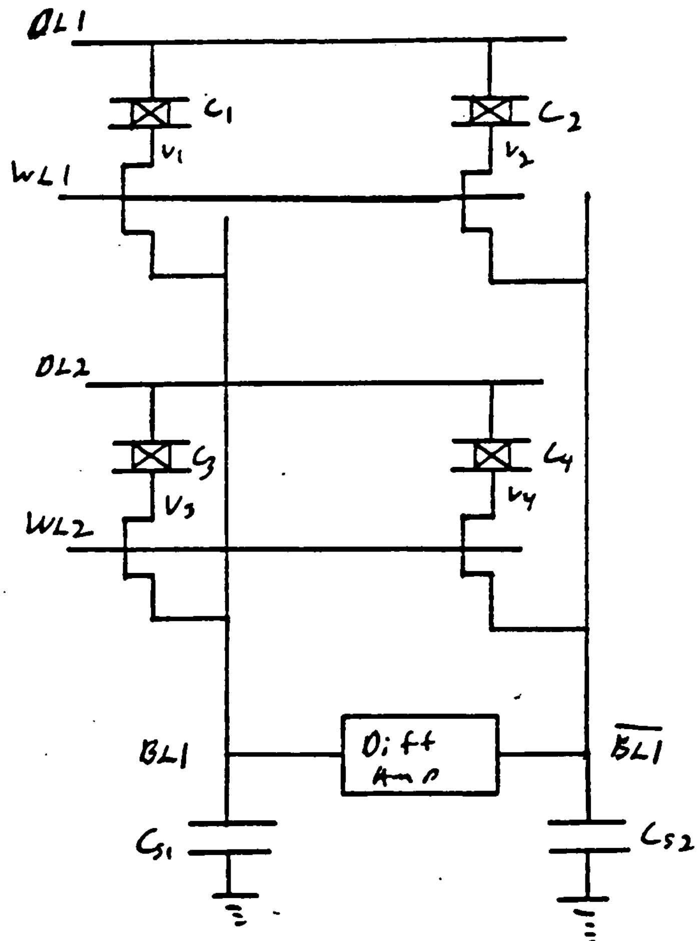

Figure 11

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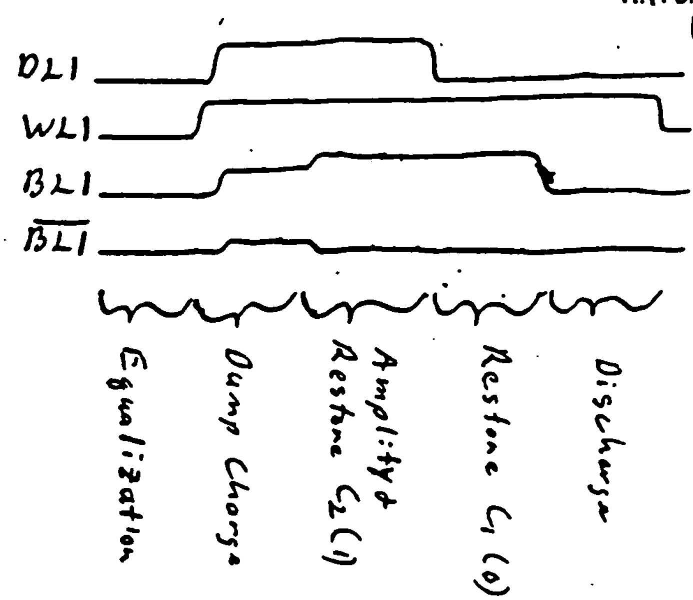

Figure 12

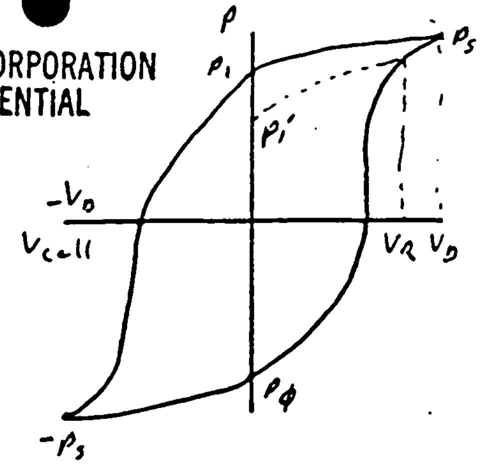

Figure 13

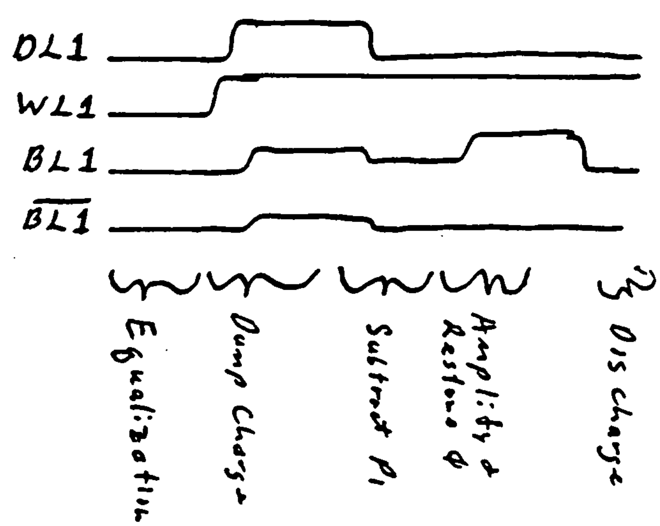

Figure 14

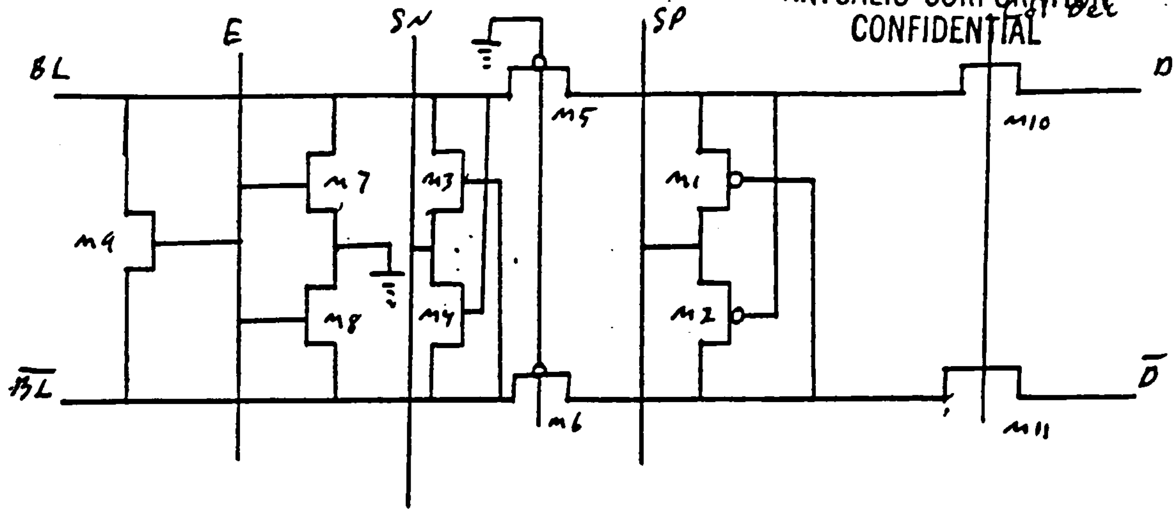

Figure 15

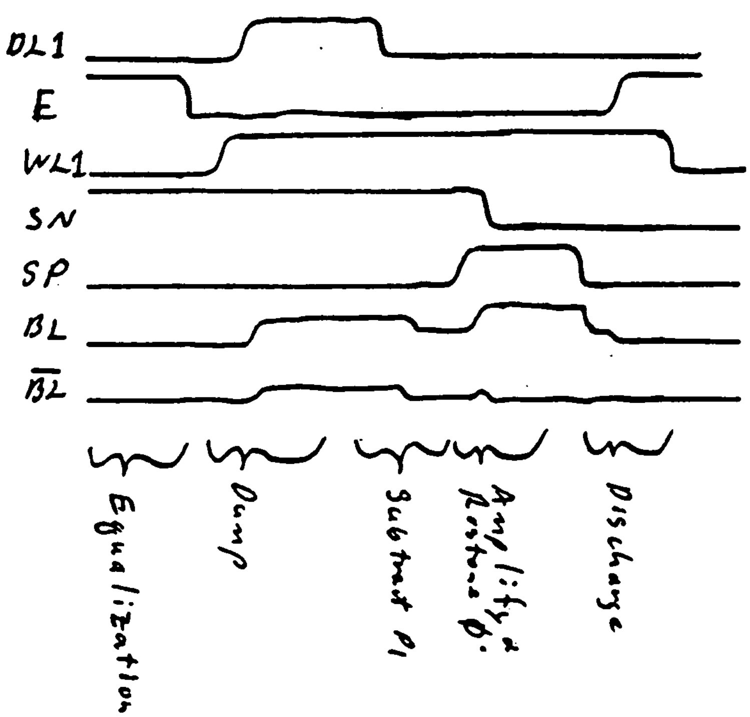

Figure 16
(For Fig 15)

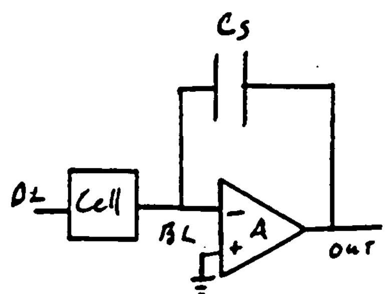

Figure 17

B

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DALLAS TELEX 73-0471
CABLE ADDRESS "RHM PATENT" DALLAS
TELECOPIER-214-742-6734

TELECOPIER INFORMATION SHEET

DATE: March 10, 1987 **CLIENT ID:** KRYS

NUMBER OF PAGES: 7 **FILE NO:** B-24,314
(INCLUDING INFORMATION SHEET)

FROM: Dale Nixon

TO: Joseph T. Evans, Jr.

FIRM NAME: Krysalis Corporation

CITY, STATE: Albuquerque, NM

BUSINESS PHONE: 505-345-1953

==

TRANSMITTING TO:
(NAME AND TYPE OF TELECOPIER)

TELECOPIER PHONE NUMBER: 505-344-8155 **GROUP I, II, III**
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Sharon Chandler
OPERATOR

IF YOU DO NOT RECEIVE ALL OF THE PAGES INDICATED, PLEASE CALL THE FOLLOWING NUMBER AS SOON AS POSSIBLE: 214-742-8013, EXT. 271.

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CABLE ADDRESS "RHM PATENT" DALLAS
TELECOPIER-214-742-6734

March 10, 1987

Mr. Joseph T. Evans, Jr.
Krysalis Corporation
4200 Osuna, NE, Suite 102
Albuquerque, NM 87109

<u>VIA TELECOPY</u>

Re: Patent Drawings for Ferroelectric Capaciter Memory System (KRYS B-24,314)

Dear Joe:

Please review the enclosed drawings which I have prepared for the subject patent application. I have taken this from your various figures, notes and comments. However, there are a number of sections that I am not certain are correct as I have drawn them. Figure 2 is the single ended circuit and the corresponding wave forms for write and read are in Figures 3 and 4. Figure 5 is the double ended circuit with the corresponding write and read wave forms in Figures 6 and 7. Finally, I have included a simple sense amp in Figure 8.

Please check each of these schematics, Figures 2 and 5, to ensure that they are accurate. Further, also check each of the wave forms to make sure that it is an accurate representation of the operation of the circuit. By including these wave forms, we do not have to show the circuits that actually generate them. I would assume all of these are being generated by some form of decoder circuit.

Please correct these figures, make any notes or comments on them, and return them to me and I can complete the drafting of the patent application.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Dale Nixon

Enclosures

C

March 23, 1987

Mr. Joseph T. Evans
Krysalis Corporation
4200 Osuna, N.E., Ste. 102 (Box 106)
Albuquerque, NM 87109

VIA FEDERAL EXPRESS

Re: NONVOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT (Our File KRYS B-24314)

Dear Joe:

Enclosed is a draft of the subject patent application, together with a set of drawings. I have selected the drawings from the set that you provided to me. These have now been sent to my draftsman to be cleaned up and placed in patent format.

I have understood most of the application, but the only part that now confuses me is in reference to Figures 11 and 12. You told me over the telephone that there was an optional turn off of the sense amplifiers. I have modified the drawings to have two vertical lines showing the turn off points, but I am not sure that I placed the turn off of the word line or even the dotted lines in the proper locations. Please review these two figures and the accompanying text to ensure that they are accurate.

There are a number of other places in the text where I had questions and I just left those questions in the text to be filled in by you.

As of now I have written in the basic independent claims and I will fill out a family of dependent claims after our first review. I think that both the apparatus and the method claims are important. I have apparatus claims for a basic read and

write circuit, the read aspect and the write aspect. I also have method claims going to both reading and writing, as well as independently for reading and writing. I think that each one of these independent claim variations approaches a different aspect of the invention. I will also include in the apparatus and method claims the aspect of automatic restoration, which I feel is an important part of the invention.

After you have had an opportunity to review the specification, claims and drawings, please mark them up, particularly the drawings, and either return them to me or call me on the phone with the changes.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Dale B. Nixon

DBN:cp

Dale,

I have included timing sheet corrections for some of the figures in the patent and I have made another figure for you to explain the READ/MODIFY/WRITE function. To do the READ/MODIFY/WRITE function requires a new level of signal complexity so bear with me in trying to understand it.

READ/MODIFY/WRITE means that the microprocessor reads a datum from a particular location with the intention of modifying its value and rewriting it back into the same location. It is a specific type of instruction in the microprocessor because the chip enable and address lines remain the same during the entire operation. The only change to the memory chip signals is that the write enable line drops after the READ to signal the memory that a word is coming back to the same address. This addressing mode is peculiar to dynamic RAMs and static RAMs do not have it. We look like a static RAM on the outside but function like a dynamic RAM on the inside so we felt we should support this mode. The dedicated READ/MODIFY/WRITE operation in the memory is shorter than doing a simple READ followed by a seperate WRITE. This is done by leaving the sense amps on while the chip is selected so they do not have to be turned on again for the WRITE. This saves maybe 20 nanoseconds.

The primary concern we have over our memory is reliability over ten years and 10^{15} cycles. The concern is over ferroelectric fatigue rates which are affected by both applied DC voltages and pulses. We have designed the signal control of the memory to limit the application of DC voltages and minimize the pulse width to give the memory its longest possible lifetime before the ferroelectric fatigues below a useful signal level. One way to eliminate the DC voltages is to ensure that zero volts are applied across the storage capacitors before the Word Line is turne off so no non-remnant charge creating a DC field is trapped in the capacitor as in a DRAM. Also, the application of forward and reverse voltages should be for the same time.

When the write enable line is active (low) when the chip enable line drops (becomes active), the memory knows that the function is a WRITE and can proceed accordingly. However, when the write enable line is high (meaning a READ operation) when the chip enable line falls, the memory does not know if the function to be performed is a READ or a READ/MODIFY/WRITE. Therefore, after the READ functio has been performed, the memory must leave to sense amps on while the chip is selected in case the microprocessor wants to write into the same location it just read from. To prevent DC aging of the ferroelectric capacitors, the capacitors and their bit lines must be isolated from the sense amps after the rewrite has taken place. This can be done with the isolation pass gates of the sense amps and the equalization transistors. Whenever the memory is not actively reading or writing, the sense amps need to be isolated from the bit lines and the equalization transistors need to be on to pull both bit lines to zero volts. With the Drive Line also at zero volts, the word line can stay on with no ill effects since there is no net voltage across either of the storage capacitors.

In analyzing the timing diagrams of the memory and sense amps, a distinction must be made between the bit lines of the memory array and the corresponding data lines of the sense amps. With the word lines, sense amps, isolation, and equalization on, the bit lines can be at zero while the data lines of the sens amps are actively holding the last data read without a DC bias being applied across the storage capacitors.

This also allows another unique invention in that the (output/input stage) and (memory decode, drive, capacitor array, and sense amps) can be decoupled so that the output stage is reading out the last data word retrieved from the array while the array is actively driving the next data word to be retrieved. This pipelining of internal functions can allow for roughly doubling the actual memory access speed over the standard access timing shown in the invention disclosure. The same can be done with the WRITE function. To take advantage of this pipelining, multiple WRITEs or READs must be done. The first access takes the standard amount of time to complete, but each subsequent access can take half the time using the pipelining technique.

Call me as I am sure this explanation is somewhat confusing.

E

April 8, 1987

Mr. Joseph T. Evans, Jr.
Krysalis Corporation
4200 Osuna, N.E., Ste. 102 (Box 106)
Albuquerque, NM 87109

Re: NONVOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT (Our File KRYS B-24314)

Dear Joe:

Enclosed is a revised draft of the subject patent application, including a new set of drawings. Please review this material and mark it up appropriately. Further, I need to have the name, address, county and citizenship of the appropriate inventor.

A further question arises in reference to FIGURE 2 and FIGURE 5. This is on page 13 of the application. The decoder and driver circuits 46 applies either a low state on the drive line or a high state on the drive line, depending upon the desired data state to be written into the capacitor 22. However, in an earlier conversation you indicated that this circuit did not receive the data input from the terminal 62 for the decoder 60. How can this circuit determine whether to produce a high or low state for writing into the capacitor 22 unless it receives that data state? But this is different from in FIGURE 10 where the drive line always goes to a positive pulse no matter whether a data 1 or a data 0 state is being written. Is this consistent between the two figures and circuits?

A further input that I need regards the use of the two times for the sense amplifier. This is in reference to FIGURE 11, in particular, the lines 128 and 130. I understand that sensing during the time 130 provides a greater operation. However, I cannot recall the trade off. What is the liability for doing so? I have left a blank for entering this information.

In regard to the above discussion of the drive line, the correction may be that we need to change the drive line for the data 1 in FIGURE 5. It is a flat line in this example, but it may need to be a pulse.

I have put in several options of operating the sense amplifier, but we may want even more. For example, should we show optional states in FIGURES 6 and 7?

I further need to know the significance of the additional vertical dotted lines at FIGURE 11.

Should we show the word lines in FIGURES 14, 15 and 16?

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Dale B. Nixon

DBN:cp

Enclosure

file

Exhibit F

May 5, 1987

Mr. Joseph T. Evans
Krysalis Corporation
4200 Osuna, N.E., Ste. 102 (Box 106)
Albuquerque, NM 87109

VIA FEDERAL EXPRESS

Re: (Our File KRYS B-24314)

Dear Joe:

Enclosed is the completed patent application for the ferroelectric memory circuit. I have revised the text and drawings according to the comments that were provided by you and by Richard. I have also made minor editorial changes to the specification. I have further added a number of claims. Please have Richard read the new claims, as well as review the full text and drawings.

After this application has been reviewed, please have Richard sign where indicated by the signature flags. The Assignment document should be notarized.

I am further including a small entity status document which we can file to reduce the filing fees by 50%. This should be signed by you and it has been made out for your signature. Please review it just to ensure that it is correct.

After all of the documents have been signed, please return them to me and I will have them filed in the Patent and Trademark Office. It is my plan to file all three applications at the same time.

Should you have any questions, please do not hesitate to contact me.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Dale B. Nixon

DBN:cp
Enclosures

6

May 12, 1987

Mr. Joseph T. Evans, Jr.
Krysalis Corporation
4200 Osuna, N.E., Ste. 102
Albuquerque, NM 87109

<u>VIA FEDERAL EXPRESS</u>

Re: Ferroelectric Capacitor Memory Circuit
(Our File KRYS B-24314)

Dear Joe:

Enclosed are the text and formal drawings for this patent application.

I will fax the final set of claims down on Wednesday.

After you and Richard have reviewed this case, please sign the original formal documents which I sent to you, including the Declaration, Assignment and the small entitiy status letter. After these have been signed, please return the complete application to me and I will see that it is filed in the Patent and Trademark Office.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Dale B. Nixon

DBN:cp

Enclosure

H

May 13, 1987

Mr. Joseph T. Evans, Jr.
Krysalis Corporation
4200 Osuna N.E., Ste. 102 (Box 106)
Albuquerque, NM 87109

Re: NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT (Our File KRYS B-24314)

Dear Joe:

Enclosed is the completed patent application for this invention. I have now completed the full set of claims and they are so extensive that it would be very time consuming to send them via fax. Also, I have made minor changes to the specification, so it is better to send a complete copy rather than trying to put pieces together. I have also included the new claims as well.

Therefore, please put together this new application and drawings, together with the formal papers which I previously sent. Please have Richard sign these papers after he has reviewed the application, including the claims, and return them to me.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK & ANDREWS

Dale B. Nixon

DBN:cp

Enclosures

I

May 28, 1987

Mr. Joseph T. Evans, Jr.
Krysalis Corporation
4200 Osuna, N.E., Ste. 102, Box 106
Albuquerque, NM 87109

VIA FEDERAL EXPRESS

Re: Non-Volatile Memory Circuit Using Ferroelectric Capacitor Storage Element
(Our File KRYS B-24314)

Dear Joe:

Enclosed is the final draft of the patent application. I have received the formal drawings which include the corrections that we recently discussed in our telephone conversation. I have further added each of the claims that we discussed at that time.

Please review the application and claims again together with Richard. Should you find any typos or small errors, please make note of them in a separate document and these can be corrected in an amendment.

After you and Richard have reviewed the application, each of you should sign the oath and declaration where indicated and the assignment where indicated. The assignment must also be notarized for each signature. In addition Joe, you should sign the statement of small entity so that we can have reduced filing fees.

After the two of you have signed the application, please forward it to Bill for his review and signature. Please ask him to then forward it to me and I will attach the necessary checks and postcards for filing in the Patent Office. It is my understanding that the schedule is to forward it to Bill on Friday and then he will get it back to me on Monday and I will have it filed on Monday.

Should you have any questions about the application, or any other matter, please do not hesitate to contact me.

Very truly yours,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

ORIGINAL SIGNED BY
DALE B. NIXON

Dale B. Nixon

DBN:cp

Enclosures

J

June 2, 1987

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

VIA EXPRESS MAIL

Re: NON-VOLATILE MEMORY CIRCUIT USING
FERROELECTRIC CAPACITOR STORAGE ELEMENT
(Our File KRYS B-24314)

Dear Sir:

Enclosed for filing are the following papers relating to Non-Volatile Memory Circuit Using Ferroelectric Capacitor Storage Element, Joseph T. Evans, Jr., William D. Miller and Richard H. Womack, inventors:

1. Specification;

2. Combined Declaration and Power of Attorney;

3. Informal Drawings (6 sheets); and

4. Check in the amount of $1,194.00.

Respectfully submitted,

RICHARDS, HARRIS, MEDLOCK
& ANDREWS

Attorneys for Applicant

ORIGINAL SIGNED BY
DALE B. NIXON

By______________________
Dale B. Nixon
Reg. No. 28,454

DBN:cp
Enclosures

PTO-103X
(Rev. 11-86)

FILING RECEIPT

B-24314
AC9
DBN

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

K

SERIAL NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
07/057,100	06/02/87	233	$1,194.00	KRYSB-24314	6	60	14

RICHARDS, HARRIS, MEDLOCK & ANDREWS
1501 ELM ST.,STE. 4500
DALLAS, TX 75270-2197

Receipt is acknowledged of the patent application identified herein. It will be considered in its order and you will be notified as to the examination thereof. Be sure to give the U.S. SERIAL NUMBER, DATE OF FILING, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this transmittal.

Applicant(s) JOSEPOH T. EVANS JR., ALBUQUERQUE, NM; WILLIAM D. MILLER, RIO RANCHO, NM; RICHARD H. WOMACK, ALBUQUERQUE, NM.

FOREIGN FILING LICENSE GRANTED 07/07/87
TITLE
NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

PRELIMINARY CLASS: 365

Docket Card SSX
Wrapper ✓ Agenda
Reference
Copies to:

RECEIVED
JUL 13 1987
RICHARDS, HARRIS, MEDLOCK
& ANDREWS

(see reverse)

L

RICHARDS, HARRIS, MEDLOCK & ANDREWS
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214-939-4500

MARCH 25, 1987

3/17/87	ADDITIONAL CLAIMS	
3/18/87	LETTER TO KRYSALIS RE APPLICATION	
	PROFESSIONAL SERVICES	$ 1,222.00

DISBURSEMENTS

2/16/87	LD CALL DLH/LEE CHAPIN	.90
3/04/87	DLH TRAVEL AND EXPENSES TO ALBUQUERQUE	188.40
3/25/87	PHOTOSTATIC COPIES	4.80
3/25/87	ONE PENCIL DRAWING	25.00
	REIMBURSABLE EXPENSES	$ 219.10

TOTAL FOR THIS MATTER $ 1,441.10 *

****

B24314 FERROELECTRIC CAPACITOR MEMORY CIRCUIT

3/06/87	FURTHER DRAFTING OF "UNICELL" PATENT APPLICATION
3/16/87	REVIEW OF DISCLOSURE MATERIAL; TELECON WITH JOE EVANS AND DRAFTING OF PATENT APPLICATION
3/19/87	FURTHER DRAFTING OF PATENT APPLICATION FOR NONVOLATILE MEMORY CIRCUIT
3/20/87	DRAFTING OF SPECIFICATION AND CLAIMS AND REVISION OF DRAWINGS FOR PATENT APPLICATION FOR NONVOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR

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MARCH 25, 1987

3/22/87	FURTHER DRAFTING OF PATENT APPLICATION FOR FERROELECTRIC CAPACITOR MEMORY CIRCUIT		
3/23/87	DRAFTING OF PATENT APPLICATION SPECIFICATION, CLAIMS AND LAYOUT OF DRAWINGS FOR FERROELECTRIC CAPACITOR MEMORY CIRCUIT		
	PROFESSIONAL SERVICES	$ 2,160.00	

DISBURSEMENTS

3/10/87	TELECOPIER SERVICE	14.00	
3/25/87	PHOTOSTATIC COPIES	2.80	
	REIMBURSABLE EXPENSES	$ 16.80	
	TOTAL FOR THIS MATTER		$ 2,176.80 *

****

Z22667 MISCELLANEOUS CORRESPONDENCE

3/04/87	MEETING IN ALBUQUERQUE AT KRYSALIS WITH JOE EVANS, BILL MILLER AND OTHERS REGARDING NEW DISCLOSURES AND SCHEDULING OF PATENT PROSECUTION		
3/24/87	PROVIDING PATENT COPIES		
	PROFESSIONAL SERVICES	$ 329.00	

DISBURSEMENTS

1/26/87	LD CALL DRN/EVANS	.50

M

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APRIL 24, 1987

KRYS

824314 FERROELECTRIC CAPACITOR MEMORY CIRCUIT

4/06/87	FURTHER DRAFTING OF PATENT APPLICATION FOR FERROELECTRIC CAPACITOR MEMORY CIRCUIT AND SYSTEM
4/07/87	FURTHER DRAFTING OF CLAIMS AND SPECIFICATION FOR FERROELECTRIC CAPACITOR MEMORY CIRCUIT AND SYSTEM
4/08/87	FURTHER DRAFTING OF PATENT APPLICATION FOR FERROELECTRIC CAPACITOR MEMORY SYSTEM

PROFESSIONAL SERVICES $ 1,344.00

DISBURSEMENTS

2/17/87	LD CALL DBW/J. EVANS	.55
3/03/87	LD CALL DBW/J. EVANS	.75
3/10/87	LD CALL DBW/505-344-8155	1.15
3/16/87	LD CALL DBW/J. EVANS	7.20
3/23/87	FEDERAL EXPRESS SERVICE	24.00
4/03/87	FOUR SHEETS, INFORMAL DRAWINGS	200.00
4/08/87	FOUR SHEETS, REVISE AND FINALIZE DRAWINGS AND TWO ADDITIONAL SHEETS, LAYOUT AND FINALIZE	125.00
4/08/87	FEDERAL EXPRESS SERVICE	24.00
4/24/87	PHOTOSTATIC COPIES	6.00

REIMBURSABLE EXPENSES $ 388.65

TOTAL FOR THIS MATTER $ 1,732.65 *

****

RICHARDS, HARRIS, MEDLOCK & ANDREWS

IMPORTANT: TO INSURE PROPER BILLING CREDIT, PLEASE DETACH AND RETURN THE TOP OF PAGE 1 WITH YOUR REMITTANCE.

N

RICHARDS, HARRIS, MEDLOCK & ANDREWS
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MAY 22, 1987

KRYS

824314 FERROELECTRIC CAPACITOR MEMORY CIRCUIT

5/05/87	REVISING APPLICATION TO INCLUDE ADDITIONAL ASPECTS AND NEW CLAIMS
5/06/87	DRAFTING OF ADDITIONAL CLAIMS FOR PATENT APPLICATION
5/07/87	FURTHER DRAFTING OF PATENT APPLICATION
5/12/87	FURTHER DRAFTING OF PATENT APPLICATIONS, SPECIFICALLY ADDING ADDITIONAL INDEPENDENT CLAIMS TO COVER MORE CONCEPTS OF CIRCUIT
5/13/87	DRAFTING OF STILL FURTHER CLAIMS TO COVER MORE ASPECTS OF FERROELECTRIC CAPACITOR MEMORY CIRCUIT
5/14/87	TELECON WITH JOE EVANS TO DISCUSS INVENTORSHIP ISSUE
5/18/87	TELECON WITH JOE EVANS TO RECEIVE REVISIONS AND MODIFICATIONS FOR PATENT APPLICATION

PROFESSIONAL SERVICES $ 3,050.00

DISBURSEMENTS

5/06/87	TELECOPIER SERVICE	20.00
5/07/87	TELECOPIER SERVICE	20.00
5/11/87	SIX SHEETS, REVISIONS TO FORMAL DRAWINGS	75.00
5/19/87	PENCIL DRAWINGS - SIX SHEETS, REVISIONS TO FORMAL DRAWINGS	30.00

RICHARDS, HARRIS, MEDLOCK & ANDREWS
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
4500 RENAISSANCE TOWER
1201 ELM STREET
DALLAS, TEXAS 75270-2197
214-939-4500

MAY 22, 1987

KRYS

5/22/87	PHOTOSTATIC COPIES	3.40	
	REIMBURSABLE EXPENSES	$ 148.40	
	TOTAL FOR THIS MATTER		$ 3,204.40

****

Z22667 MISCELLANEOUS CORRESPONDENCE

DISBURSEMENTS

4/30/87	TELECOPIER SERVICE	6.00	
	REIMBURSABLE EXPENSES	$ 6.00	
	TOTAL FOR THIS MATTER		$ 6.00

****

CURRENT TOTAL	$ 3,986.45
PREVIOUS BALANCE	$ 10,151.80
CURRENT RECEIPTS	$ 7,189.32
DUE AND PAYABLE ON RECEIPT	$ 6,948.93

PAID SINCE DATE OF STATEMENT 2962.48

ADJUSTED TOTAL DUE 3986.45

RICHARDS, HARRIS, MEDLOCK & ANDREWS

IMPORTANT: TO INSURE PROPER BILLING CREDIT, PLEASE DETACH AND RETURN THE TOP OF PAGE 1 WITH YOUR REMITTANCE.

RICHARDS, HARRIS, MEDLOCK & ANDREWS
A PROFESSIONAL CORPORATION
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214-939-4500

0

JUNE 25, 1987

KRYS

B24314 FERROELECTRIC CAPACITOR MEMORY CIRCUIT

5/28/87 DRAFTING OF ADDITIONAL CLAIMS; REVIEW OF APPLICATION IN PREPARATION FOR FILING; PREPARATION OF FORMAL PAPERS AND FORWARDING TO ALBUQUERUQE FOR SIGNATURE

PROFESSIONAL SERVICES $ 640.00

DISBURSEMENTS

5/05/87	FEDERAL EXPRESS SERVICE	24.00
5/05/87	LD CALL DBN/R. WOMACK	3.85
5/12/87	FEDERAL EXPRESS SERVICE	24.00
5/13/87	FEDERAL EXPRESS SERVICE	24.00
5/18/87	LD CALL DBN/EVANS	.10
5/29/87	LD CALL DBN/EVANS	.40
6/01/87	PATENT OFFICE FILING FEE	1,194.00
6/25/87	PHOTOSTATIC COPIES	2.20

REIMBURSABLE EXPENSES $ 1,272.55

TOTAL FOR THIS MATTER $ 1,912.55 *

****

B24854 MULTI-LAYER FERROELECTRIC CAPACITOR

DISBURSEMENTS

6/25/87	PHOTOSTATIC COPIES	19.20

REIMBURSABLE EXPENSES $ 19.20

TOTAL FOR THIS MATTER $ 19.20 *

****

RICHARDS, HARRIS, MEDLOCK & ANDREWS

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